Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (previously presented): A charge pump circuit, comprising:

a) a plurality of charge pump stages connected in series,

b) each stage of said plurality of stages containing a first auxiliary device to precharge a voltage to a gate of a charge transfer device and a second auxiliary device to switch a substrate voltage of said charge transfer device,

c) said each stage clocked by two clocks signals.

Claim 2 (previously presented): The circuit of claim 1, wherein said first and second auxiliary devices and said charge transfer devices are N-channel MOS devices contained within a P-well within a deep N-well on a P-substrate.

Claim 3 (previously presented): The circuit of claim 2, wherein said each stage further comprises a pull-down device to prevent a charge backflow between an output and an input of said each stage.

Claim 4 (previously presented): The circuit of claim 3, wherein said pull-down device is an N-channel MOSFET device that can reside either within said P-well within the deep N-well or on said P-substrate.

Claim 5 (previously presented): The circuit of claim 1, wherein each stage further comprises:

a) a first capacitor connecting a first clock signal of said two clocks signals to a gate of said charge transfer device and a gate of said second auxiliary device,

b) a second capacitor connecting a second clock signal of said two clocks signals to a gate of said first auxiliary device and an output of said charge transfer device.

Claim 6 (previously presented): The circuit of claim 1, wherein each stage that is adjacent to a first stage of said plurality of stages is clocked by said two clocks signals that are timed to be out of phase from the two clocks signals for the first stage.

Claim 7 (previously presented): The circuit of claim 1, wherein a first stage of said plurality of stages is clocked by said two clocks signals that are a first and second clock signal and stages adjacent to said first stage are clocked by the two clock signals that are a third and fourth clock signal.

Claim 8 (previously presented): The circuit of claim 1, wherein the first auxiliary device boosts an input voltage to said stage and couples the boosted voltage to a gate of the charge transfer device.

Claim 9 (previously presented): The circuit of claim 1, wherein the second auxiliary device buffers a drain of the charge transfer device from a P-well and a deep N-well of said triple well.

Claim 10 (previously presented): The circuit of claim 9, wherein said second auxiliary device reduces a body effect on said charge transfer device by transferring a boosted drain voltage of the charge transfer device to the P-well and the deep N-well.

Claim 11 (currently amended): The circuit of claim 10, wherein when said second auxiliary device is off, the P-well and the deep N-well are not coupled to any voltage source and float with a body voltage being kept in a reverse bias condition.

Claim 12 (previously presented): The circuit of claim 1, wherein said each stage is isolated by a separate and unique triple well.

Claim 13 (previously presented): The circuit of claim 1, wherein the charge transfer device and the first and second auxiliary devices are P-channel MOSFET devices residing in an N-well within a deep P-well on an N-substrate.

Claim 14 (previously presented): A circuit for pumping charge in a low voltage environment, comprising:

a) a means for coupling a plurality of stages of charge pump circuits,

b) a means for isolating devices between stages of said plurality of stages,

c) a means for transferring a boosted charge from an input to an output of each stage of said plurality of stages,

d) a means for precharging an input of a charge transferring device of said each stage,

e) a means for switching a substrate voltage of said charge transferring device of said each stage.

Claim 15 (previously presented): The circuit of claim 14, wherein the means for coupling the plurality of stages of said charge pump circuits is by serially connecting an output of a charge transferring device in a first stage to a boosting device and to said charge transferring device of a second stage.

Claim 16 (previously presented): The circuit of claim 14, wherein the means for isolating devices between said plurality of stages is by enclosing said devices of each stage within a triple well unique to each stage.

Claim 17 (previously presented): The circuit of claim 14, wherein the means for transferring said boosted charge between the input and output of each stage further comprises;

a) a first N-channel MOSFET device to produce said output,

b) a second N-channel MOSFET device which boosts said input to a gate of said first N-channel device,

c) a third N-channel MOSFET device for reducing a semiconductor body effect on said first N-channel MOSFET device.

Claim 18 (previously presented): The circuit of claim 17, further comprises a means for preventing backflow between the output and the input of said each stage of said plurality of stages.

Claim 19 (previously presented): The circuit of claim 17, wherein the second N-channel device boosts said input by coupling the input at a drain of said first N-channel device to a gate of the first N-channel device.

Claim 20 (previously presented): The circuit of claim 19, wherein the third N-channel device reduces a semiconductor body effect on said charge transferring device by coupling a boosted drain voltage of the charge transferring device to a triple well within which the charge transferring device resides.

Claim 21 (previously presented): The circuit of claim 17, wherein the first, second and third devices are P-channel MOSFET residing in an N-well within a deep P-well on an N-substrate.

Claim 22 (previously presented): A method for creating a high voltage using a charge pump circuit, comprising:

a) precharging a gate of a first charge transfer device in a first charge pump stage,

b) switching a voltage of a substrate of said first charge transfer device in said first stage to reduce a body effect of said substrate of said charge transfer device of the first stage,

c) clocking said first charge transfer device to store a boosted charge of an input of said first stage into a first capacitor to form an output of said first stage,

d) coupling said output of said first stage to the input of a second stage,

e) precharging a gate of a second charge transfer device in a second charge pump stage,

f) switching the voltage of the substrate of said second charge transfer device in said second stage to reduce a body effect of said substrate of said charge transfer device of the second stage,

g) clocking a second charge transfer device in said second stage to store said boosted charge of said input to said second stage into a second capacitor,

h) coupling said output of said second stage to the input of a next stage.

Claim 23 (previously presented): The method of claim 22, wherein said second charge transfer device is clocked off when said first charge transfer device is clocked to store said boosted charge, and said first charge transfer device is clocked off when said second charge transfer device is clocked to store said boosted charge.

Claim 24 (previously presented): The method of claim 22, wherein said boosted charge is created at said output of said first and second stages with the assist of a

precharge voltage applied to the charge transfer device and a switching of a voltage of the substrate of the charge transfer device to reduce a body effect of said substrate.

Claim 25 (previously presented): The method of claim 22 further comprising of an additional stage connected in series with the output of the second stage and performing in like manner to the first and second stages.

Claim 26 (previously presented): A negative high voltage charge pump circuit, comprising:

a) a charge transfer MOS device and an auxiliary MOS device connected together in a P-well to form a negative high voltage charge pump circuit,

b) said P-well residing in a deep N-well which is coupled to a positive voltage,

c) said deep N-well residing on a P-substrate which is coupled to ground,

d) a clock coupled to said charge transfer MOS device and to said auxiliary device through a coupling capacitor,

e) an input of said negative high voltage charge pump circuit connected to a source of the charge transfer MOS device,

f) an output of said negative high voltage charge pump circuit produced at a drain of the charge transfer MOS device.

Claim 27 (previously presented): The circuit of claim 26, wherein the charge transfer MOS device and the auxiliary MOS device are coupled together by connecting

together the drains and gates of both the charge transfer device and the auxiliary device.

Claim 28 (previously presented): The circuit of claim 26, wherein the source of the auxiliary device is connected to the P-well and thereby reducing body effects by coupling a boosted output of charge transfer device to the P-well.

Claim 29 (previously presented): The circuit of claim 26, wherein said deep N-well contains additional negative high voltage charge pump circuits.

Claim 30 (previously presented): The circuit of claim 29, wherein said additional negative high voltage charge pump circuits are connected to said output in a serial fashion to create a negative high output voltage.

Claim 31(previously presented): A circuit for pumping a negative high voltage, comprising:

a) a means for clocking each stage of a plurality of stages of a negative charge pump circuit,

b) a means for transferring a boosted negative charge from an input circuit to an output circuit of said plurality of stages,

c) a means for coupling said boosted negative charge of each pump stage of said plurality of pump stages to a P-well associated with said each pump stage.

Claim 32 (previously presented): The circuit of claim 31, further comprising a means for containing said P-well of each stage within a common deep N-well, and wherein a positive voltage is coupled to said deep N-well.

Claim 33 (previously presented): The circuit of claim 31, wherein said means for transferring a boosted
negative charge is controlled by clocking a first stage with a clock signal that is out of phase with said clock signal of a second stage that is connected to said first stage.

Claim 34 (previously presented): A method of creating a high voltage negative charge pump, comprising:

a) coupling a plurality of negative charge pump stages together in a serial fashion,

b) coupling an input of a first charge pump stage to a source of a charge transfer device.

c) coupling a drain of the charge transfer device to an output of said first charge pump stage.

d) coupling the output of the first charge pump stage to drain of an auxiliary device in said first charge pump stage and to said input of a second charge pump stage,

e) coupling the source of said auxiliary device to a P-well containing said first charge pump stage,

f) coupling a clock signal to a circuit node comprising a connection between gates and drains of the charge transfer device and the auxiliary device.

Claim 35 (previously presented): The method of claim 34, wherein coupling the source of the auxiliary device to the P-well couples a boosted charge to the P-well, thereby reducing body effects on the output of said charge pump stage contained within said P-well.

Claim 36 (previously presented): The method of claim 34, wherein coupling said clock signal connected to said circuit node in said first charge pump stage is out of phase with said clock signal connected to said circuit node in said second charge pump stage.

Claim 37 (previously presented): The method of claim 34, wherein the second charge pump stage is contained within a separate P-well from the P-well of the first charge pump stage.

Claim 38 (previously presented): The method of claim 34, wherein a plurality of said negative charge pump stages are contained within a plurality of P-wells which reside in a deep N-well on a P-substrate.